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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,055	03/16/2004	Takuya Yasui	L8462.04109	1194

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EXAMINER	
MERANT, GUERRIER	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/18/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,055	YASUI ET AL.	
	Examiner	Art Unit	
	Guerrier Merant	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 20040316.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is the initial office action based on the application filed on March 16, 2004. Claims 1-9 are currently pending and have been considered below.

Claim Objections

2. Claim 7 is objected to because of the following informalities:

In the last four lines of 7, " the power supply" should be "a power supply".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Okamura (US 5,521,541)** and further in view of **Skergan et al. (US 6,452,435 B1)**.

4. Claims 1 and 8: **Okamura** discloses a semiconductor integrated circuit *(item 200; Fig. 2)*, comprising: a plurality of flip-flop circuits *(item 106, Fig. 2)* being operated by a clock signal for normal operation during a normal operation *(col. 3, lines 7-12)*, respectively, a clock circuit for normal operation for transmitting said clock signal for normal operation to said flip-flop circuit wherein said clock circuit has a lattice-shaped wiring portion, and supplies said clock signal taken out of said lattice-shaped wiring

portion to said flip-flop circuit *(col. 2, lines 64-67 & col. 3, lines 1-27).* But **Okamura** fails to disclose a scan chain to be operated by a clock signal for scan during a scan test. However, **Skergan et al.** discloses a method and apparatus for scanning and clocking chips with high-speed free running clock in a manufacturing test environment wherein *clock controls 220, 225, and 230 are used to control the internal scanning and clocking of the chip when in a test mode. In a preferred embodiment, Stop_En 220 is used to prevent the mesh clock from clocking the functional devices of the circuit while in the LSSD test mode. Whenever Stop_En 220 is low, a system clock pulse is generated at the output of the local clock buffer for each rising edge of Test_Clk 215. Test_Clk 215 is the LSSD test clock that is sourced by the manufacturing tester under the control of test patterns. When not in the test mode, Stop_En 220 is always high and the mesh clock propagates through local clock buffers 260 ungated (col. 3, lines 18-29).* Therefore at the time of the invention, one of ordinary skill in the art would have found it obvious *to incorporate the LSSD circuit disclosed in* **Skergan et al.** *in order to test the chip at speed while also allowing the expensive test equipment, which is currently in use to be utilized to perform such testing. Also one would have found it obvious to require only one tightly tuned high-speed clock distribution system because of the added complexity and increase wiring that results from the use of multiple clock distribution systems.*

5. Claim 2: **Okamura** and **Skergan et al.** discloses a semiconductor integrated circuit as in claim1 above, wherein the flip-flop circuits are arranged in the interior and the neighborhood region of the lattice-shaped wiring portion of the clock circuit for scan

(item 106, see fig. 2 for location; ***Okamura****)*, and wherein said clock circuit for scan has a external clock input terminal for scan for inputting the clock signal for scan, inputs the clock signal for scan which is transmitted from said external clock input terminal for scan to the center of said lattice-shaped wiring portion, and takes out the clock signal for scan from a predetermined location of said lattice-shaped wiring portion, respectively, to supply it to each said flip-flop circuit *(col. 3, lines 3-17;* **Skergan et al.** *)*.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Okamura** and **Skergan et al.** as applied to claim 1 above, and further in view of **Godfrey et al. (US 6,550,031 B1)**.

7. Claim 3: **Okamura** and **Skergan et al.** discloses a semiconductor integrated circuit as in claim above 1, but fail to disclose a selector circuit arranged to each flip-flop circuit, and wherein said selector circuit inputs the clock signal for normal operation which is transmitted through the clock circuit for normal operation and the clock signal for scan which is transmitted through the clock circuit for scan, selects said clock signal for normal operation during the normal operation to output it to said flip-flop circuit, and selects said clock signal for scan during the scan test to output it to said flip-flop circuit. However, **Godfrey et al.** discloses *a clock circuit wherein a multiplexer (item 415; Fig. 5)* is used to *provide a system clock to latches 402, 403 when the microcontroller M is in a normal mode. When the microcontroller M is in a scan mode, a SCAN_MODE signal is provided to the multiplexer 415, and the multiplexer 415 can provide a CLK_SCAN*

signal to latches 402, 403 (col. 7, lines 13-19). Therefore at the time of the invention, one of ordinary skill in the art would have found it obvious to incorporate the clock circuit of **Godfrey et al.** with the semiconductor of **Okamura** and **Skergan et al.** to use different test modes while testing the integrated circuits.

8. Claim 4: **Okamura** and **Skergan et al.** discloses a semiconductor integrated circuit as in claim 1 above, wherein the clock circuit for normal operation is configured so that transmission paths of the clock signal for normal operation may become in a tree-shape *(col.2, lines1-57).*

Claim 5: **Okamura** and **Skergan et al.** discloses a semiconductor integrated circuit as in claim 1 above, wherein there are a plurality of types of clock signals for normal operation *(see item 120;* **Skergan et al.***)* which are transmitted through the clock circuit for normal operation, and any one type of said clock signals for normal operation among the plurality of types thereof is supplied to each flip-flop circuit which configures the scan chain and said clock signal for normal operation of the same type is supplied to said flip-flop circuits which synchronize during the normal operation, and wherein said clock circuit for normal operation is configured so that transmission paths of the clock signal for normal operation for each type may become in the tree-shape *(col. 2, lines 1-67;* **Skergan et al.***)*.

9. Claims 6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Okamura** and **Skergan et al.** as applied to claim 1 above, and further in view of **Mc Elvain et al. (US 2006/0095872 A1)**.

Claims 6 and 9: **Okamura** and **Skergan et al.** discloses a semiconductor integrated circuit as in claim 1 above, wherein the clock circuit for scan has a external clock input terminal for scan for inputting the clock signal for scan, and connects the driver element which drives said lattice-shaped wiring portion between said external clock input terminal for scan and the lattice-shaped wiring portion *(col. 3, lines 3-17;* **Skergan et al.** *)*. But **Okamura** and **Skergan et al.** fail to disclose a power supply wiring of said driver element wider in width and has a lower resistance compared with a power supply wiring of an element which configures the clock circuit for normal operation. However, **McElvain et al.** discloses *methods and apparatuses to design an Integrated Circuit (IC) with a shielding of wires. In at least one embodiment, a shielding mesh of at least two reference voltages (e.g., power and ground) is used to reduce both the capacitive coupling and the inductive coupling in routed signal wires in IC chips (see abstract).* And *each of the subset of wires is substantially wider than the third plurality of signal wires so that the subset of wires forms a power ring that reduces the impedance in the shielding mesh caused by the window in shielding mesh [0025].* Therefore at the time of the invention, one of ordinary skill in the art would have found it obvious to use the method teaching in **McElvain et al.** in the integrated circuits of **Okamura** and **Skergan et al.** in order to reduce power consuming.

10. Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Okamura** and **Skergan et al.** as applied to claim 1 above, and further in view of **Meier et al. (US 5,854,567).**

11. Claim 7: **Okamura** and **Skergan et al.** discloses a semiconductor integrated circuit as in claim 1 above, wherein the clock circuit for scan has a external clock input terminal for scan to which the clock signal for scan is inputted, and connects the driver element which drives said lattice-shaped wiring portion between said external clock input terminal for scan and the lattice-shaped wiring portion *(col. 2, lines 1-57 & col. 3, lines 3-17;* **Skergan et al.***)*. But **Okamura** and **Skergan et al.** fail to disclose a power supply voltage of said driver element is made lower than the power supply voltage of the element which configures the clock circuit for normal operation. However, **Meier et al.** discloses *a clock circuit for an integrated circuit which reduces power consumption achieved by an integrated circuit arrangement having a clock driver circuit, a first terminal of at least a last stage of the clock driver circuit being supplied with a clock supply voltage that is lower in terms of amount than a general supply voltage of the integrated circuit, whereby a second terminal of the at least one last stage of the clock driver circuit is directly connected to reference potential, and whereby a load current flows between the first and second terminal (col. 2, lines 1-23).* Therefore at the time of the invention, one of ordinary skill in the art would have been motivated to include the

clock system of **Meier et al.** in the integrated circuits of **Okamura** and **Skergan et al.** in order to lower power consumption and minimize testing costs.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a) **Narayanan et al. (US 5,774,474)** discloses a high speed scan testing vacillated by pipelining or distributing a scan enable signal to scan circuits through a distributing network.

b) **Mitra et al (US 5,668,490) :**"Flip-flop with full scan capability"

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady, can be reached on (571) 272-3819. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Merant Guerrier
12/06/06

ALBERT DECADY
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